FPL 25 Reading List

Highlighting Significant Contributions from 25 Years of the International Conference on Field Programmable Logic and Applications (1991–2014)

The first International Conference on Field-Programmable Logic and Applications (FPL) was held in 1991 at Oxford University. In the ensuing years, it has become the largest meeting on field-programmable gate array (FPGA) technologies and systems, and many important contributions have been published at the conference. Below are listed the most significant contributions from 1991 to 2014. The selection was made by an international Significant Papers Committee (SPC), as described in this article, where the endorsements are detailed.

1993

Dynamic reconfiguration of FPGAs
Patrick Lysaght and John Dunlop
Dynamic Reconfiguration

1995

An assessment of the suitability of FPGA-based systems for use in digital signal processing
Russell J. Petersen, Brad L. Hutchings
Applications and Benchmarks

1996

RaPiD - reconfigurable pipelined datapath
C. Ebeling, D.C. Cronquist and P. Franklin
Architecture

A virtual hardware operating system for the Xilinx XC6200
C. Ebeling, D.C. Cronquist, P. Franklin
Dynamic Reconfiguration

1997

VPR: A new packing, placement and routing tool for FPGA research
Vaughn Betz and Jonathan Rose
Design Methods and Tools

1999

SONIC - a plug-in architecture for video processing Simon D. Haynes, Peter Y. K. Cheung, Wayne Luk, John Stone
Applications and Benchmarks

2000

Multitasking on FPGA Coprocessors
Harald Simmler, L. Levinson and Reinhard Männer
Applications and Benchmarks

Stream Computations Organized for Reconfigurable Execution (SCORE)
Eylon Caspi, Michael Chu, Randy Huang, Joseph Yeh, John Wawrzynek and André DeHon
Architecture

StReAm: Object-Oriented Programming of Stream Architectures Using PAM-Blox
Oskar Mencer, Heiko Hübert, Martin Morf and Michael J. Flynn
Design Methods and Tools

2002

A Flexible Power Model for FPGAs
Kara K. W. Poon, Andy Yan, Steven J. E. Wilton
Architecture

Granidt: Towards Gigabit Rate Network Intrusion Detection Technology
Maya Gokhale, Dave Dubois, Andy Dubois, Mike Boorman, Steve Poole, Vic Hogsett
Security and Network-on-Chip

2003

A Smith-Waterman Systolic Cell
Chi Wai Yu, K. H. Kwong, Kin-Hong Lee, Philip H. W. Leong
Applications and Benchmarks

ADRES: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix
Bingfeng Mei, Serge Vernalde, Diederik Verkest, Hugo De Man, Rudy Lauwereins

Architecture

Virtualizing Hardware with Multi-context Reconfigurable Arrays
Rolf Enzler, Christian Plessl, Marco Platzner
Dynamic Reconfiguration

Networks on Chip as Hardware Components of an OS for Reconfigurable Systems
Théodore Marescaux, Jean-Yves Mignolet, Andrei Bartic, W. Moffat, Diederik Verkest, Serge Vernalde, Rudy Lauwereins
Security and Network-on-Chip

Fast, Large-Scale String Match for a 10Gbps FPGA-Based Network Intrusion Detection System
Ioannis Sourdis, Dionisios N. Pnevmatikatos
Security and Network-on-Chip

2004

A Dual-VDD Low Power FPGA Architecture
Aman Gayasen, K. Lee, Narayanan Vijaykrishnan, Mahmut T. Kandemir, Mary Jane Irwin, Tim Tuan
Architecture

The Impact of Pipelining on Energy per Operation in Field-Programmable Gate Arrays
Steven J. E. Wilton, Su-Shin Ang and Wayne Luk
Design Methods and Tools

2005

Context Saving and Restoring for Multitasking in Reconfigurable Systems
Heiko Kalte and Mario Porrmann
Dynamic Reconfiguration

2006

Enhanced Architectures, Design Methodologies and CAD Tools for Dynamic Reconfiguration of Xilinx FPGAs
Patrick Lysaght, Brandon Blodget, Jeff Mason, Jay Young and Brendan Bridgford
Design Methods and Tools

2007

Physical Unclonable Functions, FPGAs and Public-Key Crypto for IP Protection
Jorge Guajardo, Sandeep S. Kumar, Geert Jan Schrijena and Pim Tuyls

Applications and Benchmarks

2008

ReCoBus-Builder - A novel tool and technique to build statically and dynamically reconfigurable systems for FPGAs

Dirk Koch, Christian Beckhoff and Jürgen Teich
Dynamic Reconfiguration

2009

Performance comparison of FPGA, GPU and CPU in image processing

Shuichi Asano, Tsutomu Maruyama and Yoshiki Yamaguchi
Applications and Benchmarks

FPGA partial reconfiguration via configuration scrubbing

Jonathan Heiner, Benjamin Sellers, Michael J. Wirthlin and Jeff Kalb
Dynamic Reconfiguration

2010

FPGA Implementations of the Round Two SHA-3 Candidates

Brian Baldwin, Andrew Byrne, Liang Lu, Mark Hamilton, Neil Hanley, Mire O'Neill, William P. Marnane
Applications and Benchmarks

2013

Accelerating Solvers for Global Atmospheric Equations Through Mixed-Precision Data Flow Engine

Lin Gan, Haohuan Fu, Wayne Luk, Chao Yang, Wei Xue, Xiaomeng Huang, Youhui Zhang, Guangwen Yang
Applications and Benchmarks

The Power of Communication: Energy-Efficient NoCs for FPGAs

Mohamed Abdelfattah and Vaughn Betz
Security and Network-on-Chip

Revision #3
Created 8 September 2024 19:20:47 by Suhaib Fahmy (Admin)
Updated 18 September 2024 19:54:19 by Suhaib Fahmy (Admin)