FPGA 20 Reading List

Highlighting Significant Contributions from 20 Years of the International Symposium on Field-Programmable Gate Arrays (1992–2011)

For the 20th anniversary of the International Symposium on Field-Programmable Gate Arrays in 2012, we have assembled a special volume to highlight the most significant papers from the conferences. We highlight 25 papers across all years and major FPGA topics that best exemplify the contributions from the conference. Compared to the 400–500 papers that have appeared in the conference, 25 papers will represent roughly 5% of all the papers published in the conference to date.

Listed below are the 25 papers. Linked for each paper is a one-page endorsement written by an expert in the field that captures the historical context in which the paper was written and offers a retrospective view on its significance. A URL link to the original paper is provided at the bottom of each endorsement.

1994

Unifying FPGAs and SIMD Arrays
Michael Bolotski, André DeHon, Thomas F. Knight, Jr.
Architecture

Endorsement by: Jonathan Rose

1995

PathFinder: A Negotiation-Based Performance-Driven Router for FPGAs
Larry McMurchie and Carl Ebeling
Computer-Aided Design

Endorsement by Sinan Kaptanoglu

Simultaneous Depth and Area Minimization in LUT-based FPGA Mapping
Jason Cong and Yean-Yow Hwang

Computer-Aided Design

Endorsement by Eugene Ding

1996

DPGA Utilization and Application
André DeHon
Applications

Endorsement by John Wawrzynek

1997

Signal Processing at 250 MHz using High-Performance FPGA's
Brian Von Herzen
Applications

Endorsement by André DeHon and Steve Trimberger

1998

A survey of CORDIC algorithms for FPGA based computers
Ray Andraka
Applications

Endorsement by Paul Chow

Managing Pipeline-Reconfigurable FPGAs
Srihari Cadambi, Jeffery Weener, Seth Copen Goldstein, Herman Schmit, Donald E. Thomas
Reconfigurable Computing

Endorsement by Katherine Compton and André DeHon

1999

Balancing Interconnect and Computation in a Reconfigurable Computing Array (or, why you don't really want 100% LUT utilization)
André DeHon
Architecture

Endorsement by Mike Hutton

Cut Ranking and Pruning: Enabling a General and Efficient FPGA Mapping Solution
Jason Cong, Chang Wu, Yuzheng Ding
Computer-Aided Design

Endorsement by Steve Wilton

FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density
Vaughn Betz, Jonathan Rose

Architecture

Endorsement by Carl Ebeling

HSRA: High-Speed, Hierarchical Synchronous Reconfigurable Array
William Tsu, Kip Macy, Atul Joshi, Randy Huang, Norman Walker, Tony Tung, Omid Rowhani, Varghese George, John Wawrzynek, André DeHon
Architecture

Endorsement by Carl Ebeling

Using Cluster-Based Logic Blocks and Timing-Driven Packing to Improve FPGA Speed and Density
Alexander (Sandy) Marquardt, Vaughn Betz, Jonathan Rose
Computer-Aided Design

Endorsement by Steve Wilton

2000

Automatic Generation of FPGA Routing Architectures from High-Level Descriptions
Vaughn Betz, Jonathan Rose
Computer-Aided Design

Endorsement by Scott Hauck

The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density
Elias Ahmed, Jonathan Rose
Architecture

Endorsement by Mike Hutton

Timing-Driven Placement for FPGAs
Alexander (Sandy) Marquardt, Vaughn Betz, Jonathan Rose
Computer-Aided Design

Endorsement by Jason Cong

2001

Using Sparse Crossbars within LUT Clusters
Guy Lemieux, David Lewis
Architecture

Endorsement by Sinan Kaptanoglu

2002

Dynamic Power Consumption in Virtex™-II FPGA Family
Li Shang, Alireza Kaviani, Kusuma Bathala
Circuits

Endorsement by Russ Tessier

On the Sensitivity of FPGA Architectural Conclusions to Experimental Assumptions, Tools, and Techniques
Andy Yan, Rebecca Cheng, Steven J.E. Wilton
Architecture

Endorsement by Katherine Compton

2003

The Stratix™ Routing and Logic Architecture
David Lewis, Vaughn Betz, David Jefferson, Andy Lee, Chris Lane, Paul Leventis, Sandy Marquardt, Cameron McClintock, Bruce Pedersen, Giles Powell, Srinivas Reddy, Chris Wysocki, Richard Cliff, Jonathan Rose
Architecture

Endorsement by Herman Schmit

2004

Active Leakage Power Optimization for FPGAs
Jason H. Anderson, Farid N. Najm, Tim Tuan
Circuits

Endorsement by Russ Tessier

FPGAs vs. CPUs: Trends in Peak Floating-Point Performance
Keith Underwood
Reconfigurable Computing

Endorsement by Paul Chow

Nanowire-Based Sublithographic Programmable Logic Arrays
André DeHon, Michael J. Wilson
Architecture

Endorsement by Deming Chen

2006

Measuring the Gap Between FPGAs and ASICs
Ian Kuon, Jonathan Rose
Architecture

Endorsement by Herman Schmit

2008

High-Quality, Deterministic Parallel Placement for FPGAs on Commodity Hardware
Adrian Ludwin, Vaughn Betz, Ketan Padalia
Computer-Aided Design

Endorsement by Jonathan Rose

2010

Efficient Multi-Ported Memories for FPGAs
Charles Eric LaForest, J. Gregory Steffan
Applications

Endorsement by Scott Hauck

Foreword and all endorsements as a single PDF

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