Hall of Fame Inductees

Below are papers that have been inducted into the TCFPGA Hall of Fame. Nominations are secured each year, followed by detailed consideration by a panel of experts. The papers inducted to date appear below:

Class of 2026

DAOmap: A Depth-optimal Area Optimization Mapping Algorithm for FPGA Designs
Deming Chen and Jason Cong
Proceedings of IEEE/ACM International Conference on Computer-Aided Design, 2004
Inducted at the IEEE Symposium on Field-Programmable Custom Computing Machines, 15th May 2026

(endorsement)

Class of 2025

Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks
Chen Zhang, Peng Li, Guangyu Sun, Yijin Guan, Bingjun Xiao, Jason Cong
Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2015, pp. 161–170.
Inducted at the ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 28th February 2025

(endorsement)

Class of 2024

Designing custom arithmetic data paths with FloPoCo
Florent De Dinechin, Bogdan Pasca
IEEE Design and Test, Vol. 28, No. 4, pp. 18–27, 2011
Inducted at the International Conference on Field Programmable Logic and Applications, 5th September 2024

Class of 2023

Application-Specific Instruction Generation for Configurable Processor Architectures
Jason Cong, Y. Fan, G. Han, Zhiru Zhang
Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2004, pp. 183-189.
(

endorsement)

JBits: Java based interface for reconfigurable computing

Steve Guccione, Delon Levi and Prasanna Sundararajan

Proceedings of the 2nd Annual Military and Aerospace Applications of Programmable Devices and Technologies Conference, 1999.

(endorsement)

Class of 2022

Improving FPGA Performance and Area Using an Adaptive Logic Module

Mike Hutton, Jay Schleicher, David Lewis, Bruce Pedersen, Richard Yuan, Sinan Kaptanoglu, Gregg Baeckler, Boris Ratchev, Ketan Padalia, Mark Bourgeault , Andy Lee, Henry Kim and Rahul Saini

14th Field Programmable Logic, 2004, pp. 135-144

(endorsement)

FCUDA: Enabling efficient compilation of CUDA kernels onto FPGAs

Alexandros Papakonstantinou, Karthik Gururaj, John A. Stratton, Deming Chen, Jason Cong, Wen-Mei W. Hwu

IEEE Symposium on Application Specific Processors, 2009, pp. 35-42

(endorsement)

An efficient and versatile scheduling algorithm based on SDC formulation

Jason Cong and Zhiru Zhang

Design Automation Conference, 2006, pp. 433-438

(endorsement)

Class of 2021

Performance-Constrained Pipelining of Software Loops onto Reconfigurable Hardware

Greg Snider

International Symposium on FPGAs, Feb. 2002, Pages 177–186

inducted at the International Symposium on Field-Programmable Gate Arrays on March 2, 2021

(endorsement)

Directional and Single-Driver Wires in FPGA Interconnect

Guy Lemieux, Edmund Lee, Marvin Tom, and Anthony Yu

2004 IEEE International Conference on Field-Programmable Technology, December 2004, Pages 41-48

Inducted at the International Conference on Field-Programmable Technology on December 9, 2021

(endorsement)

Class of 2020

ReconOS: Multithreaded Programming for Reconfigurable Computers
Enno Lübbers and Marco Platzner
IEEE Transactions on Embedded Computing Systems (TECS), Volume: 9, Issue: 1, October 2009

High-Quality, Deterministic Parallel Placement for FPGAs on Commodity Hardware
Adrian Ludwin, Vaughn Betz and Ketan Padalia
Proceedings of the 16th International ACM/SIGDA Symposium on Field Programmable Gate Arrays, pp 14–23, February 2008

(endorsement)

Class of 2019

The Density Advantage of Configurable Computing
André DeHon
IEEE Computer, Volume: 33 , Issue: 4, pp. 41–49, April 2000

(endorsement)

A High-performance Microarchitecture with Hardware-programmable Functional Units
Rahul Razdan and Michael. D. Smith
roceedings of the 27th Annual International Symposium on Microarchitecture, pp. 172–180, Nov/Dec 1994

(endorsement)

Processor reconfiguration through instruction-set metamorphosis
Peter M. Athanas and Harvey F. Silverman
IEEE Computer, Volume 26, Issue 3, pp 11–18, March 1993

(endorsement)

Class of 2018

A User Programmable Reconfigurable Logic Array
William S. Carter, Khue Duong, Ross H. Freeman, Hung-Cheng Hsieh, Jason Y. Ja, John E. Mahoney, Luan T. Ngo, Shelly L. Sze
Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 233–235, 1986

(endorsement)

An Efficient Logic Emulation System
Joseph Varghese, Michael Butts, and Jon Batcheller
IEEE Transactions on VLSI Systems, vol. 1, no. 2, pp. 171–174, June 1993

(endorsement)

Building and Using a Highly Parallel Programmable Logic Array

Maya Gokhale, William Holmes, Andrew Kopser, Sara Lucas, Ronald Minnich, Douglas Sweely and Daniel Lopresti

IEEE Computer, vol. 24, no. 1, pp. 81–89, Jan. 1991

(endorsement)

Class of 2017

FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs

Jason Cong and Yuzheng Ding

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 13, no. 1, pp. 1-12, Jan 1994

(endorsement)

Programmable Active Memories: Reconfigurable Systems Come of Age

Jean E. Vuillemin, Patrice Bertin, Didier Roncin, Mark Shand, Hervé Touati, and Philippe Boucard

IEEE Transactions on Very Large Scale Integration Systems, vol. 4, no. 1, pp. 56–69, March 1996

(endorsement)

A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology

James R. Heath, Philip J. Kuekes, Gregory S. Snider, and R. Stanley Williams

Science, 12 Jun 1998, vol. 280, no. 5370, pp. 1716-1721

(endorsement)

FPGA 20, FCCM 20, and FPL25 Class

All papers from the FPGA 20, FCCM 20, and FPL 25 lists are also inductees in the Hall of Fame

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