FPT Best Paper Awards

The International Conference on Field Programmable Technology (FPT) has awarded Best Paper Awards to the following papers:

2025, Shanghai, China

JEDI-Linear: Fast and Efficient Graph Neural Networks for Jet Tagging on FPGAs
Zhiqiang Que, Chang Sun, Sudarshan Paramesvaran, Emyr Clement, Katerina Karakoulaki, Christopher Brown, Lauri Laatu, Arianna Cox, Alexander Tapper, Wayne Luk and Maria Spiropulu

2024, Sydney, Australia

GraphNoC: Graph Neural Networks for Application-Specific FPGA NoC Performance Prediction
Gurshaant Malik and Nachiket Kapre

2023, Yokohama, Japan

PolyLUT: Learning Piecewise Polynomials for Ultra-Low Latency FPGA LUT-based Inference
Marta Andronic and George A. Constantinides

Into the Third Dimension: Architecture Exploration Tools for 3D Reconfigurable Acceleration Devices
Andrew Boutros, Fatemehsadat Mahmoudi, Amin Mohaghegh, Stephen More and Vaughn Betz

2022, Hong Kong SAR

Cloning the Unclonable: Physically Cloning an FPGA RO PUF
Hayden Cook, Jonathan Thompson, Zephram Tripp, Brad Hutchings and Jeffrey Goeders

2021, Virtual Conference

A High-Performance and Flexible FPGA Inference Accelerator for Decision Forests Based on Prior Feature Space Partitioning
Thiem Van Chu, Ryuichi Kitajima, Kazushi Kawamura, Jaehoon Yu and Masato Motomura

2019, Tianjin, China

Partitioning FPGA-Optimized Systolic Arrays for Fun and Profit
Long Chung Chan, Gurshaant Malik and Nachiket Kapre

2018, Naha, Japan

Dither NN: An Accurate Neural Network with Dithering for Low Bit-Precision Hardware
Kota Ando, Kodai Ueyoshi, Yuka Oba, Kazutoshi Hirose, Ryota Uematsu, Takumi Kudo, Masayuki Ikebe, Tetsuya Asai, Shinya Takamaeda-Yamazaki and Masato Motomura

2017, Melbourne, Australia

Synthesis of Program Binaries into FPGA Accelerators with Runtime Dependence Validation
Shaoyi Cheng, Qijing Huang and John Wawrzynek

2016, Xian, China

High Density, Low Energy, Magnetic Tunnel Junction Based Block RAMs for Memory-rich FPGAs
Kosuke Tatsumura, Sadegh Yazdanshenas and Vaughn Betz

2015, Queenstown, New Zealand

Energy Minimization in the Time-Space Continuum
Hyunseok Park, Shreel Vijayvargiya and André DeHon

2014, Shanghai, China

Design Re-Use for Compile Time Reduction in FPGA High-Level Synthesis Flows
Marcel Gort and Jason Anderson

2013, Kyoto, Japan

Maximum Flow Algorithms for Maximum Observability During FPGA Debug
Eddie Hung, Al-Shahna Jamal and Steven J. E. Wilton

2012, Seoul, South Korea

iDEA: A DSP Block Based FPGA Soft Processor
Hui Yan Cheah, Suhaib A. Fahmy and Douglas L. Maskell

Graph Minor Approach for Application Mapping on CGRAs
Liang Chen; Tulika Mitra

2011, New Delhi, India

VLIW-SCORE: Beyond C for Sequential Control of SPICE FPGA Acceleration
Nachiket Kapre and André DeHon

2010, Beijing, China

Parallelizing FPGA placement using transactional memory
Steven Birk. J. Gregory Steffan and Jason H. Anderson

2009, Sydney, Australia

American Option Pricing on Reconfigurable Hardware Using Least-Squares Monte Carlo Method
Xiang Tian and Khaled Benkrid

2008, Taipei, Taiwan

Optimizing Residue Arithmetic on FPGAs
Haohuan Fu, Oskar Mencer and Wayne Luk

2007, Kitakyushu, Japan

Memory Footprint Reduction For FPGA Routing Algorithms
Scott Y.L. Chin and Steven J.E. Wilton

2006, Bangkok, Thailand

FPGA core watermarking based on power signature analysis
Daniel Ziener and Jurgen Teich

2005, Singapore

Dynamic voltage scaling for commercial FPGAs
C.T. Chow, L.S.M. Tsui, Philip H.W. Leong, Wayne Luk; Steven J.E. Wilton

2004, Brisbane, Australia

Directional and Single-Driver Wires in FPGA Interconnect

Guy Lemieux; Edmund Lee; Marvin Tom; Anthony Yu

2003, Tokyo, Japan

Product Term Embedded Synthesizable Logic Cores

Andy Yan and S.J.E. Wilton

Source

Revision #6
Created 2024-09-18 14:39:44 UTC by Suhaib Fahmy (Admin)
Updated 2026-03-21 11:38:17 UTC by Suhaib Fahmy (Admin)