FPL Best Paper Awards

The International Conference on Field Programmable Logic and Applications (FPL) awards three awards:

Michal Servit Memorial Award (MS) awarded to the most outstanding paper in the area of design algorithms, methods, and CAD tools for FPGAs and self-aware systems.

Stamatis Vassiliadis Memorial Award (SV) awarded to the most outstanding paper in the area of Architecture & Applications.

FPL Community Award awarded to those who have made a significant contribution to the community by providing some material or knowledge in an open format that benefits the rest of the community.

FPL has awarded the awards:

2026, Ghent, Belgium

MS: **FPGA Acceleration of Fully Homomorphic Encryption with Adaptive Key Switching**
Zhihan Xu, Jayashree Adivarahan, Rajgopal Kannan, and Viktor Prasanna

SV: **Cocotb-PYNQ-PR: From Co-Simulation to Deployment — A Unified DFX Framework for PYNQ**
Emir Guevara, Chaitanya Sharma, Gavin Lusby, and Nachiket Kapre

Community: **Dynamatic: An Open-Source HLS Compiler That Generates Dynamically Scheduled Circuits from C/C++ Code**
Lana Josipović, Paolo Ienne, and the entire Dynamatic team

2025, Leiden, The Netherlands

MS: **From Errors to Solutions: LLM-Powered Command Scripting for FPGA CAD Tools**
Mohamed A. Elgammal and Vaughn Betz

SV: **Double Duty: FPGA Architecture to Enable Concurrent LUT and Adder Chain Usage**
Xilai Dai, Junius Pun, Grace Zgheib, Mahesh Iyer, Andrew Boutros, Vaughn Betz and Mohamed Abdelfattah

Community: **Koios: A Deep Learning Benchmark Suite for FPGA Architecture and CAD Research**
Aman Arora, Andrew Boutros, Daniel Rauch, Aishwarya Rajen, Aatman Borda, Seyed Alireza

Damghani, Samidh Mehta, Sangram Kate, Pragnesh Patel, Kenneth B. Kent, Vaughn Betz and Lizy K. John

2024, Turin, Italy

MS: **DynaRapid: Fast-Tracking from C to Routed Circuits**
Andrea Guerrieri, Srijeet Guha, Chris Lavin, Eddie Hung, Lana Josipovic and Paolo Ienne

SV: **SERI: High-Throughput Streaming Acceleration of Electron Repulsion Integral Computation in Quantum Chemistry using HBM-based FPGAs**
Philip Stachura, Guanyu Li, Xin Wu, Christian Plessl and Zhenman Fang

Community: **Artifact Evaluation Initiative**
Miriam Leeser and Suhaib Fahmy

2023, Gothenburg, Sweden

MS: **Compiler Discovered Dynamic Scheduling of Irregular Code in High-Level Synthesis**
Robert Szafarczyk, Syed Waqar Nabi and Wim Vanderbauwhede

SV: **Co-ViSu: a Video Super-Resolution Accelerator Exploiting Codec Information Reuse**
Haishuang Fan, Jingya Wu, Wenyan Lu, Xiaowei Li and Guihai Yan

Commmunity: **GNNBuilder: An Automated Framework for Generic Graph Neural Network Accelerator Generation, Simulation, and Optimization**
Stefan Abi-Karam and Cong Hao

2022, Belfast, United Kingdom

MS: **Bitfiltrator: A general approach for reverse-engineering Xilinx bitstream format**
Sahand Kashani, Mahyar Emami and James R. Larus

SV: **DeLiBA: An Open-Source Hardware/Software Framework for the Development of Linux Block I/O Accelerators**
Babar Khan, Carsten Heinz and Andreas Koch

2021, Virtual Conference

MS: **Turning PathFinder Upside-Down: Exploring FPGA Switch-Blocks by Negotiating Switch Presence**
Stefan Nikolić and Paolo Ienne

SV: **Eciton: Very Low-Power LSTM Neural Network Accelerator for Predictive Maintenance at the Edge**
Jeffrey Chen, Sehwan Hong, Warrick He, Jinyeong Moon and Sang-Woo Jun

Community: **FGPU: An SIMT-Architecture for FPGAs** (published at FPGA 2016)
Muhammed Al Kadi, Benedikt Janssen and Michael Huebner

2020, Virtual Conference

MS: **Timing-Driven Placement for FPGA Architectures with Dedicated Routing Paths**
Stefan Nikolić, Grace Zgheib and Paolo Ienne

SV: **LogicNets: Co-Designed Neural Networks and Circuits for Extreme-Throughput Applications**
Yaman Umuroglu, Yash Akhauri, Nicholas J. Fraser and Michaela Blott

2019, Barcelona, Spain

MS: **A Deep Learning Framework to Predict Routability for FPGA Circuit Placement**
Abeer Alhyari, Ahmed Shamli, Ziad Abuwaimer, Shawki Areibi and Gary Grewal

SV: **Characterizing Power Distribution Attacks in Multi-User FPGA Environments**
George Provelengios, Daniel Holcomb and Russell Tessier

2018, Dublin, Ireland

MS: **Machine-Learning Based Congestion Estimation for Modern FPGAs**
Dani Maarouf, Abeer Alhyari, Ziad Abuowaimer, Timothy Martin, Andrew Gunter, Gary Grewal, Shawki Areibi and Anthony Vannelli

SV: **Embracing Diversity: Enhanced DSP Blocks for Low-Precision Deep Learning on FPGAs**
Andrew Boutros, Sadegh Yazdanshenas and Vaughn Betz

2017, Ghent, Belgium

SV: **Automated Generation of Banked Memory Architectures in the High-Level Synthesis of Multi-Threaded Software**
Yu Ting Chen and Jason H. Anderson

MS: **Voltage Drop-based Fault Attacks on FPGAs using Valid Bitstreams**
Dennis R. E. Gnad, Fabian Oboril and Mehdi B. Tahoori

Community: **FloPoCo Parameterized Floating-Point Core Generator**
Florent De Dinechin

2016, Lausanne, Switzerland

MS: **An Evaluation on the Accuracy of the Minimum Width Transistor Area Models in Ranking the Actual Layout Area of FPGA Architectures**
Farheen Fatima Khan and Andy Ye

SV: **An Investigation into a Circuit Based Supply Chain Analyzer for FPGAs**
Jacob Couch and John Arkoian

Community: **JetStream: An open-source high-performance PCI Express 3 streaming library for FPGA-to-Host and FPGA-to-FPGA communication**
Malte Vesper, Dirk Koch, Kizheppatt Vipin and Suhaib A. Fahmy

2015, London, United Kingdom

MS: **Hoplite: Building austere overlay NoCs for FPGAs**
Nachiket Kapre and Jan Gray

SV: **CoRAM++: Supporting Data Structure-specific Memory Interfaces for FPGA Computing**
Gabriel Weisz and James C. Hoe

Community: **Placement and routing frameworks for FPGA research**
Vaughn Betz

2014, Munich, Germany

MS: **Hardware Accelerated Novel Optical De Novo Assembly for Large-Scale Genomes**
Pingfan Meng, Matthew Jacobsen, Motoki Kimura, Vladimir Dergachev, Thomas Anantharaman, Michael Requa and Ryan Kastner

Community: **LegUp High Level Synthesis Framework**
Jason H. Anderson and Stephen Brown

2013, Porto, Portugal

MS: **A Run-Time Graph-Based Polynomial Placement and Routing Algorithm for Virtual FPGAs**
R. Ferreira, L. Rocha, A. Santos, J. Nacif, Stephan Wong and Luigi Carro

SV: **The Power of Communication: Energy-Efficient NoCs for FPGAs**
Mohamed S. Abdelfattah and Vaughn Betz

Community: **RIFFA 2.0: A Reusable Integration Framework for FPGA Accelerators**
Matthew Jacobsen and Ryan Kastner

2012, Oslo, Norway

MS: **Correctly Rounded Floating-Point Division for DSP-Enabled FPGAs**
Bogdan Pasca

SV: **Automatically Exploiting Regularity in Applications to Reduce Reconfiguration Memory Requirements**
Fatma Abouelella, Karel Bruneel and Dirk Stroobandt

Community: **A High Performance, Open Source SATA2 Core**
Ashwin A. Mendon, Bin Huang and Ron Sass

2011, Crete, Greece

Community: **RapidSmith: Do-It-Yourself CAD Tools for Xilinx FPGAs**
Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent E. Nelson and Brad L. Hutchings

2010, Milan, Italy

MS: **Enhancing FPGA Device Capabilities by the Automatic Logic Mapping to Additive Carry Chains**
Thomas B. Preusser and Rainer G. Spallek

SV: **FPGA-Optimised Uniform Random Number Generators Using LUTs and Shift Registers**
David B. Thomas and Wayne Luk

Community: **ATHENa - Automated Tool for Hardware EvaluatioN: Toward Fair and Comprehensive Benchmarking of Cryptographic Hardware Using FPGAs**
Kris Gaj, Jens-Peter Kaps, Venkata Amirineni, Marcin Rogawski, Ekawat Homsirikamol and Benjamin

Y. Brewster

2009, Prague, Czech Republic

MS: **Exploiting Fast Carry-Chains of FPGAs for Designing Compressor Trees**
Hadi Parandeh-Afshar, Philip Brisk and Paolo Ienne

2008, Heidelberg, Germany

SV: **Rapid estimation of power consumption for hybrid FPGAs**
Chun Hok Ho, Philip H.W. Leong, Wayne Luk and Steven J.E. Wilton

2007, Amsterdam, Netherlands

SV: **Domain-Specific Hybrid FPGA: Architecture and Floating Point Applications**
Chun Hok Ho, Chi Wai Yu, Philip H.W. Leong, Wayne Luk and Steven J.E. Wilton

2006, Madrid, Spain

Multi-layer Floorplanning on a Sequence of Reconfigurable Designs
Love Singhal and Elaheh Bozorgzadeh

Altera Award on FPGA Architectures: **Power Implications of Implementing Logic Using FPGA Embedded Memory Arrays**
Scott Y.L. Chin, Clarence S.P. Lee and Steven J.E. Wilton

Xilinx Award on FPGA Technology: **Reducing the Space Complexity of Pipelined Routing using Modified Range Encoding**
Allan Carroll and Carl Ebeling

More About the Awards:

Michal Servit was General Chair of FPL 1994 in Prague, the largest FPL ever held to that date. He was an associate professor at the EE dept. of the University of Prague. Michal Servit attended all FPLs, and served as a reviewer for all those years as a member of the program committee, and steering committee of FPL. Unfortunately, he did not survive a heart attack during vacations in Austria, December 5, 1997. The community misses with him as a cooperative and highly competent friend full of good ideas. He was an important part of the FPL organization. The first Michael Servit Memorial Award was initially organized by Stephen Guccione triggered by an idea from John Schewel.

Prof. Stamatis Vassiliadis (IEEE Fellow, ACM Fellow, Member of the Dutch Academy of Sciences, and Professor at Delft University of Technology), is well known as an outstanding computer scientist

and for establishing the SAMOS conference in 2001. When he passed away much too early on 7 April 2007, the community lost one of its most skilled and inspiring actors. Stamatis Vassiliadis was involved in the organization of many scientific conferences and he was the general chair of FPL2007.

The FPL Community Award was introduced at FPL 2010 in Milano by the organizers Fabrizio Ferrandi, Marco D. Santambrogio, and Jari Nurmi.

Revision #6
Created 2024-09-18 12:18:08 UTC by Suhaib Fahmy (Admin)
Updated 2026-10-06 14:21:43 UTC by Suhaib Fahmy (Admin)