

FCCM Best Paper Awards

The IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) has awarded Best Paper Awards to the following papers:

2024, Orlando, FL

[A Data-Driven, Congestion-Aware and Open-Source Timing-Driven FPGA Placer](#)

[Accelerated by GPUs](#)

Zhili Xiong, Rachel Selina Rajarathnam and David Z. Pan

Best Short Paper: **[Synthesis of LUT Networks for Random-Looking Dense Functions with Don't Cares - Towards Efficient FPGA Implementation of DNN](#)**

Yukio Miyasaka, Alan Mishchenko, Nicholas Fraser and John Wawrzynek

2023, Marina Del Rey, CA

[A Machine Learning Approach for Predicting the Difficulty of FPGA Routing Problems](#)

Andrew David Gunter and Steven J.E. Wilton

Best Paper Runner Up: **[LightningSim: Fast and Accurate Trace-Based Simulation for High-Level Synthesis](#)**

Rishov Sarkar and Cong Hao

2022, New York City, NY

[CoMeFa: Compute-in-Memory Blocks for FPGAs](#)

Aman Arora, Tanmay Anand, Aatman Borda, Rishabh Sehgal, Bagus Hanindhito, Jaydeep Kulkarni and Lizy K. John

2021, Virtual Conference

[Clockwork: Resource-Efficient Static Scheduling for Multi-Rate Image Processing Applications on FPGAs](#)

Dillon Huff, Steve Dai and Pat Hanrahan

Best Short Paper: **[ESCA: Event-Based Split-CNN Architecture with Data-Level Parallelism on UltraScale+ FPGA](#)**

Pankaj Bhowmik, Jubaer Hossain Pantho, Joel Mandebi Mbongue and Christophe Bobda

2020, Virtual Conference

[Comparison of Arithmetic Number Formats for Inference in Sum-Product Networks on FPGAs](#)

Lukas Sommer, Lukas Weber, Martin Kumm and Andreas Koch

Best Short Paper: **[Yosys+nextpnr: an Open Source Framework from Verilog to Bitstream for Commercial FPGAs](#)**

David Shah, Eddie Hung, Clifford Wolf, Serge Bazanski, Dan Gisselquist and Miodrag Milanovic

2019, San Diego, CA

[Templatified soft floating-point for High-Level Synthesis](#)

David B. Thomas

2018, Boulder, CO

[ReBNet: Residual Binarized Neural Network](#)

Mohammad Ghasemzadeh, Mohammad Samragh and Farinaz Koushanfar

Best Short Paper: **[Fast and Accurate Estimation of Quality of Results in High-Level Synthesis with Machine Learning](#)**

Steve Dai, Yuan Zhou, Hang Zhang, Ecenur Ustun, Evangeline F.Y. Young and Zhiru Zhang

2017, Napa, CA

[High-Performance Hardware Merge Sorter](#)

Susumu Mashimo, Thiem Van Chu and Kenji Kise

Best Short Paper: **[Evaluating Rapid Application Development with Python for Heterogeneous Processor-based FPGAs](#)**

Andrew G. Schmidt, Gabriel Weisz and Matthew French

2016, Washington DC

[KAPow: A System Identification Approach to Online Per-module Power Estimation in FPGA Designs](#)

Eddie Hung, James J. Davis, Joshua M. Levine, Edward A. Stott, Peter Y.K. Cheung and George A. Constantinides

Best Short Paper: [GRVI Phalanx: A Massively Parallel RISC-V FPGA Accelerator Accelerator](#)

Jan Gray

2015, Vancouver, Canada

[Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs](#)

Jeffrey Goeders and Steve J.E. Wilton

2014, Boston, MA

[Speeding Up FPGA Placement: Parallel Algorithms and Methods](#)

Matthew An, J. Gregory Steffan and Vaughn Betz

2013, Seattle, WA

[Parallel Computation of Skyline Queries](#)

Louis Woods, Gustavo Alonso and Jens Teubner

2012, Toronto, Canada

[Hardware Acceleration of Short Read Mapping](#)

Corey B. Olson, Maria Kim, Cooper Clauson, Boris Kogon, Carl Ebeling, Scott Hauck and Walter L. Ruzzo

2011, Salt Lake City, UT

[Multilevel Granularity Parallelism Synthesis on FPGAs](#)

Alexandros Papakonstantinou, Yun Liang, John A. Stratton, Karthik Gururaj, Deming Chen, Wen-Mei W. Hwu and Jason Cong

2010, Charlotte, NC

[Hardware Acceleration of Approximate Tandem Repeat Detection](#)

Tomáš Martínek and Matej Lexa

[Rapid RNA Folding: Analysis and Acceleration of the Zuker Recurrence](#)

Arpith C. Jacob, Jeremy D. Buhler and Roger D. Chamberlain

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