Community Awards

Here we collect an archive of awards that have been bestowed by conferences in our community as well to members of our community.

- FPGA Best Paper Awards
- FCCM Best Paper Awards
- FPL Best Paper Awards
- FPT Best Paper Awards
- ACM TRETS Best Paper Awards

FPGA Best Paper Awards

The ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA) has awarded Best Paper Awards to the following papers:

2024

Formal Verification of Source-to-Source Transformations for HLS
Louis-Noël Pouchet, Emily Tucker, Niansong Zhang, Hongzheng Chen, Debjit Pal, Gabriel Rodríguez and Zhiru Zhang

2023

DONGLE: Direct FPGA-Orchestrated NVMe Storage for HLS
Linus Y. Wong, Jialiang Zhang and Jing (Jane) Li

2022

RapidStream: Parallel Physical Implementation of FPGA HLS Designs
Licheng Guo, Pongstorn Maidee, Yun Zhou, Chris Lavin, Jie Wang, Yuze Chi, Weikang Qiao, Alireza Kaviani, Zhiru Zhang and Jason Cong

2021

AutoBridge: Coupling Coarse-Grained Floorplanning and Pipelining for High-Frequency HLS Design on Multi-Die FPGAs
Licheng Guo, Yuze Chi, Jie Wang, Jason Lau, Weikang Qiao, Ecenur Ustun, Zhiru Zhang and Jason Cong

2020

Buffer Placement and Sizing for High-Performance Dataflow Circuits
Lana Josipović, Shabnam Sheikhha, Andrea Guerrieri, Paolo Ienne and Jordi Cortadella

2019

HeteroCL: A Multi-Paradigm Programming Infrastructure for Software-Defined Reconfigurable Computing
Yi-Hsiang Lai, Yuze Chi, Yuwei Hu, Jie Wang, Cody Hao Yu, Yuan Zhou, Jason Cong and Zhiru Zhang

2018

FASTCF: FPGA-based Accelerator for Stochastic-Gradient-Descent-based Collaborative Filtering

Shijie Zhou, Rajgopal Kannan, Yu Min and Viktor K. Prasanna

2017

ESE: Efficient Speech Recognition Engine with Compressed LSTM on FPGA

Song Han, Junlong Kang, Huizi Mao, Yiming Hu, Xin Li, Yubin Li, Dongliang Xie, Hong Luo, Song Yao, Yu Wang, Huazhong Yang, William (Bill) J. Dally

2016

FPRESSO: Enabling Express Transistor-Level Exploration of FPGA Architectures

Grace Zgheib, Manana Lortkipanidze, Muhsen Owaida, David Novo and Paolo Ienne

2015

Take the Highway: Design for Embedded NoCs on FPGAs

Mohamed S. Abdelfattah, Andrew Bitar and Vaughn Betz

2014

Optimizing Effective Interconnect Capacitance for FPGA Power Reduction

Safeen Huda, Jason Anderson and Hirotaka Tamura

2013

Polyhedral-Based Data Reuse Optimization for Configurable Computing

Louis-Noel Pouchet, Peng Zhang, P. Sadayappan and Jason Cong

2012

Rethinking FPGAs: elude the flexibility excess of LUTs with and-inverter cones

Hadi Parandeh-Afshar, Hind Benbihi, David Novo and Paolo Ienne

2011

CoRAM: an in-fabric memory architecture for FPGA-based computing

Eric S. Chung, James C. Hoe, and Ken Mai

FCCM Best Paper Awards

The IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) has awarded Best Paper Awards to the following papers:

2024, Orlando, FL

A Data-Driven, Congestion-Aware and Open-Source Timing-Driven FPGA Placer Accelerated by GPUs
Zhili Xiong, Rachel Selina Rajarathnam and David Z. Pan

Best Short Paper: **Synthesis of LUT Networks for Random-Looking Dense Functions with Don't Cares – Towards Efficient FPGA Implementation of DNN**
Yukio Miyasaka, Alan Mishchenko, Nicholas Fraser and John Wawrzynek

2023, Marina Del Rey, CA

A Machine Learning Approach for Predicting the Difficulty of FPGA Routing Problems
Andrew David Gunter and Steven J.E. Wilton

Best Paper Runner Up: **LightningSim: Fast and Accurate Trace-Based Simulation for High-Level Synthesis**
Rishov Sarkar and Cong Hao

2022, New York City, NY

CoMeFa: Compute-in-Memory Blocks for FPGAs
Aman Arora, Tanmay Anand, Aatman Borda, Rishabh Sehgal, Bagus Hanindhito, Jaydeep Kulkarni and Lizy K. John

2021, Virtual Conference

Clockwork: Resource-Efficient Static Scheduling for Multi-Rate Image Processing Applications on FPGAs
Dillon Huff, Steve Dai and Pat Hanrahan

Best Short Paper: **ESCA: Event-Based Split-CNN Architecture with Data-Level Parallelism on UltraScale+ FPGA**

Pankaj Bhowmik, Jubaer Hossain Pantho, Joel Mandebi Mbongue and Christophe Bobda

2020, Virtual Conference

Comparison of Arithmetic Number Formats for Inference in Sum-Product Networks on FPGAs
Lukas Sommer, Lukas Weber, Martin Kumm and Andreas Koch

Best Short Paper: **Yosys+nextpnr: an Open Source Framework from Verilog to Bitstream for Commercial FPGAs**
David Shah, Eddie Hung, Clifford Wolf, Serge Bazanski, Dan Gisselquist and Miodrag Milanovic

2019, San Diego, CA

Templatised soft floating-point for High-Level Synthesis
David B. Thomas

2018, Boulder, CO

ReBNet: Residual Binarized Neural Network
Mohammad Ghasemzadeh, Mohammad Samragh and Farinaz Koushanfar

Best Short Paper: **Fast and Accurate Estimation of Quality of Results in High-Level Synthesis with Machine Learning**
Steve Dai, Yuan Zhou, Hang Zhang, Ecenur Ustun, Evangeline F.Y. Young and Zhiru Zhang

2017, Napa, CA

High-Performance Hardware Merge Sorter
Susumu Mashimo, Thiem Van Chu and Kenji Kise

Best Short Paper: **Evaluating Rapid Application Development with Python for Heterogeneous Processor-based FPGAs**
Andrew G. Schmidt, Gabriel Weisz and Matthew French

2016, Washington DC

KAPow: A System Identification Approach to Online Per-module Power Estimation in FPGA Designs
Eddie Hung, James J. Davis, Joshua M. Levine, Edward A. Stott, Peter Y.K. Cheung and George A. Constantinides

Best Short Paper: **GRVI Phalanx: A Massively Parallel RISC-V FPGA Accelerator Accelerator**
Jan Gray

2015, Vancouver, Canada

Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs
Jeffrey Goeders and Steve J.E. Wilton

2014, Boston, MA

Speeding Up FPGA Placement: Parallel Algorithms and Methods
Matthew An, J. Gregory Steffan and Vaughn Betz

2013, Seattle, WA

Parallel Computation of Skyline Queries
Louis Woods, Gustavo Alonso and Jens Teubner

2012, Toronto, Canada

Hardware Acceleration of Short Read Mapping
Corey B. Olson, Maria Kim, Cooper Clauson, Boris Kogon, Carl Ebeling, Scott Hauck and Walter L. Ruzzo

2011, Salt Lake City, UT

Multilevel Granularity Parallelism Synthesis on FPGAs
Alexandros Papakonstantinou, Yun Liang, John A. Stratton, Karthik Gururaj, Deming Chen, Wen-Mei W. Hwu and Jason Cong

2010, Charlotte, NC

Hardware Acceleration of Approximate Tandem Repeat Detection
Tomáš Martínek and Matej Lexa

Rapid RNA Folding: Analysis and Acceleration of the Zuker Recurrence
Arpith C. Jacob, Jeremy D. Buhler and Roger D. Chamberlain

FPL Best Paper Awards

The International Conference on Field Programmable Logic and Applications (FPL) awards three awards:

Michal Servit Memorial Award (MS) awarded to the most outstanding paper in the area of design algorithms, methods, and CAD tools for FPGAs and self-aware systems.

Stamatis Vassiliadis Memorial Award (SV) awarded to the most outstanding paper in the area of Architecture & Applications.

FPL Community Award awarded to those who have made a significant contribution to the community by providing some material or knowledge in an open format that benefits the rest of the community.

FPL has awarded the awards:

2024, Turin, Italy

MS: **[DynaRapid: Fast-Tracking from C to Routed Circuits](#)**
Andrea Guerrieri, Srijeet Guha, Chris Lavin, Eddie Hung, Lana Josipovic and Paolo Ienne

SV: **[SERI: High-Throughput Streaming Acceleration of Electron Repulsion Integral Computation in Quantum Chemistry using HBM-based FPGAs](#)**
Philip Stachura, Guanyu Li, Xin Wu, Christian Plessl and Zhenman Fang

Community: **Artifact Evaluation Initiative**
Miriam Leeser and Suhaib Fahmy

2023, Gothenburg, Sweden

MS: **[Compiler Discovered Dynamic Scheduling of Irregular Code in High-Level Synthesis](#)**
Robert Szafarczyk, Syed Waqar Nabi and Wim Vanderbauwhede

SV: **[Co-ViSu: a Video Super-Resolution Accelerator Exploiting Codec Information Reuse](#)**
Haishuang Fan, Jingya Wu, Wenyan Lu, Xiaowei Li and Guihai Yan

Commmunity: **[GNNBuilder: An Automated Framework for Generic Graph Neural Network Accelerator Generation, Simulation, and Optimization](#)**
Stefan Abi-Karam and Cong Hao

2022, Belfast, United Kingdom

MS: **Bitfiltrator: A general approach for reverse-engineering Xilinx bitstream format**
Sahand Kashani, Mahyar Emami and James R. Larus

SV: **DeLiBA: An Open-Source Hardware/Software Framework for the Development of Linux Block I/O Accelerators**
Babar Khan, Carsten Heinz and Andreas Koch

2021, Virtual Conference

MS: **Turning PathFinder Upside-Down: Exploring FPGA Switch-Blocks by Negotiating Switch Presence**
Stefan Nikolić and Paolo Ienne

SV: **Eciton: Very Low-Power LSTM Neural Network Accelerator for Predictive Maintenance at the Edge**
Jeffrey Chen, Sehwan Hong, Warrick He, Jinyeong Moon and Sang-Woo Jun

Community: **FGPU: An SIMT-Architecture for FPGAs** (published at FPGA 2016)
Muhammed Al Kadi, Benedikt Janssen and Michael Huebner

2020, Virtual Conference

MS: **Timing-Driven Placement for FPGA Architectures with Dedicated Routing Paths**
Stefan Nikolić, Grace Zgheib and Paolo Ienne

SV: **LogicNets: Co-Designed Neural Networks and Circuits for Extreme-Throughput Applications**
Yaman Umuroglu, Yash Akhauri, Nicholas J. Fraser and Michaela Blott

2019, Barcelona, Spain

MS: **A Deep Learning Framework to Predict Routability for FPGA Circuit Placement**
Abeer Alhyari, Ahmed Shamli, Ziad Abuwaimer, Shawki Areibi and Gary Grewal

SV: **Characterizing Power Distribution Attacks in Multi-User FPGA Environments**
George Provelengios, Daniel Holcomb and Russell Tessier

2018, Dublin, Ireland

MS: **Machine-Learning Based Congestion Estimation for Modern FPGAs**
Dani Maarouf, Abeer Alhyari, Ziad Abuowaimer, Timothy Martin, Andrew Gunter, Gary Grewal, Shawki Areibi and Anthony Vannelli

SV: **Embracing Diversity: Enhanced DSP Blocks for Low-Precision Deep Learning on FPGAs**
Andrew Boutros, Sadegh Yazdanshenas and Vaughn Betz

2017, Ghent, Belgium

SV: **Automated Generation of Banked Memory Architectures in the High-Level Synthesis of Multi-Threaded Software**
Yu Ting Chen and Jason H. Anderson

MS: **Voltage Drop-based Fault Attacks on FPGAs using Valid Bitstreams**
Dennis R. E. Gnad, Fabian Oboril and Mehdi B. Tahoori

Community: **FloPoCo Parameterized Floating-Point Core Generator**
Florent De Dinechin

2016, Lausanne, Switzerland

MS: **An Evaluation on the Accuracy of the Minimum Width Transistor Area Models in Ranking the Actual Layout Area of FPGA Architectures**
Farheen Fatima Khan and Andy Ye

SV: **An Investigation into a Circuit Based Supply Chain Analyzer for FPGAs**
Jacob Couch and John Arkoian

Community: **JetStream: An open-source high-performance PCI Express 3 streaming library for FPGA-to-Host and FPGA-to-FPGA communication**
Malte Vesper, Dirk Koch, Kizheppatt Vipin and Suhaib A. Fahmy

2015, London, United Kingdom

MS: **Hoplite: Building austere overlay NoCs for FPGAs**
Nachiket Kapre and Jan Gray

SV: **CoRAM++: Supporting Data Structure-specific Memory Interfaces for FPGA Computing**
Gabriel Weisz and James C. Hoe

Community: **Placement and routing frameworks for FPGA research**
Vaughn Betz

2014, Munich, Germany

MS: **Hardware Accelerated Novel Optical De Novo Assembly for Large-Scale Genomes**
Pingfan Meng, Matthew Jacobsen, Motoki Kimura, Vladimir Dergachev, Thomas Anantharaman, Michael Requa and Ryan Kastner

Community: **LegUp High Level Synthesis Framework**
Jason H. Anderson and Stephen Brown

2013, Porto, Portugal

MS: **A Run-Time Graph-Based Polynomial Placement and Routing Algorithm for Virtual FPGAs**
R. Ferreira, L. Rocha, A. Santos, J. Nacif, Stephan Wong and Luigi Carro

SV: **The Power of Communication: Energy-Efficient NoCs for FPGAs**
Mohamed S. Abdelfattah and Vaughn Betz

Community: **RIFFA 2.0: A Reusable Integration Framework for FPGA Accelerators**
Matthew Jacobsen and Ryan Kastner

2012, Oslo, Norway

MS: **Correctly Rounded Floating-Point Division for DSP-Enabled FPGAs**
Bogdan Pasca

SV: **Automatically Exploiting Regularity in Applications to Reduce Reconfiguration Memory Requirements**
Fatma Abouelella, Karel Bruneel and Dirk Stroobandt

Community: **A High Performance, Open Source SATA2 Core**
Ashwin A. Mendon, Bin Huang and Ron Sass

2011, Crete, Greece

Community: **RapidSmith: Do-It-Yourself CAD Tools for Xilinx FPGAs**
Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent E. Nelson and Brad L. Hutchings

2010, Milan, Italy

MS: **Enhancing FPGA Device Capabilities by the Automatic Logic Mapping to Additive Carry Chains**
Thomas B. Preusser and Rainer G. Spallek

SV: **FPGA-Optimised Uniform Random Number Generators Using LUTs and Shift Registers**
David B. Thomas and Wayne Luk

Community: **ATHENa - Automated Tool for Hardware EvaluatioN: Toward Fair and Comprehensive Benchmarking of Cryptographic Hardware Using FPGAs**
Kris Gaj, Jens-Peter Kaps, Venkata Amirineni, Marcin Rogawski, Ekawat Homsirikamol and Benjamin Y. Brewster

2009, Prague, Czech Republic

MS: **Exploiting Fast Carry-Chains of FPGAs for Designing Compressor Trees**
Hadi Parandeh-Afshar, Philip Brisk and Paolo Ienne

2008, Heidelberg, Germany

SV: **Rapid estimation of power consumption for hybrid FPGAs**
Chun Hok Ho, Philip H.W. Leong, Wayne Luk and Steven J.E. Wilton

2007, Amsterdam, Netherlands

SV: **Domain-Specific Hybrid FPGA: Architecture and Floating Point Applications**
Chun Hok Ho, Chi Wai Yu, Philip H.W. Leong, Wayne Luk and Steven J.E. Wilton

2006, Madrid, Spain

Multi-layer Floorplanning on a Sequence of Reconfigurable Designs
Love Singhal and Elaheh Bozorgzadeh

Altera Award on FPGA Architectures: **Power Implications of Implementing Logic Using FPGA Embedded Memory Arrays**
Scott Y.L. Chin, Clarence S.P. Lee and Steven J.E. Wilton

Xilinx Award on FPGA Technology: **Reducing the Space Complexity of Pipelined Routing using Modified Range Encoding**

Allan Carroll and Carl Ebeling

More About the Awards:

Michal Servit was General Chair of FPL 1994 in Prague, the largest FPL ever held to that date. He was an associate professor at the EE dept. of the University of Prague. Michal Servit attended all FPLs, and served as a reviewer for all those years as a member of the program committee, and steering committee of FPL. Unfortunately, he did not survive a heart attack during vacations in Austria, December 5, 1997. The community misses with him as a cooperative and highly competent friend full of good ideas. He was an important part of the FPL organization. The first Michael Servit Memorial Award was initially organized by Stephen Guccione triggered by an idea from John Schewel.

Prof. Stamatis Vassiliadis (IEEE Fellow, ACM Fellow, Member of the Dutch Academy of Sciences, and Professor at Delft University of Technology), is well known as an outstanding computer scientist and for establishing the SAMOS conference in 2001. When he passed away much too early on 7 April 2007, the community lost one of its most skilled and inspiring actors. Stamatis Vassiliadis was involved in the organization of many scientific conferences and he was the general chair of FPL2007.

The FPL Community Award was introduced at FPL 2010 in Milano by the organizers Fabrizio Ferrandi, Marco D. Santambrogio, and Jari Nurmi.

FPT Best Paper Awards

The International Conference on Field Programmable Technology (FPT) has awarded Best Paper Awards to the following papers:

2024, Sydney, Australia

GraphNoC: Graph Neural Networks for Application-Specific FPGA NoC Performance Prediction
Gurshaant Malik and Nachiket Kapre

2023, Yokohama, Japan

PolyLUT: Learning Piecewise Polynomials for Ultra-Low Latency FPGA LUT-based Inference
Marta Andronic and George A. Constantinides

Into the Third Dimension: Architecture Exploration Tools for 3D Reconfigurable Acceleration Devices
Andrew Boutros, Fatemehsadat Mahmoudi, Amin Mohaghegh, Stephen More and Vaughn Betz

2022, Hong Kong SAR

Cloning the Unclonable: Physically Cloning an FPGA RO PUF
Hayden Cook, Jonathan Thompson, Zephram Tripp, Brad Hutchings and Jeffrey Goeders

2021, Virtual Conference

A High-Performance and Flexible FPGA Inference Accelerator for Decision Forests Based on Prior Feature Space Partitioning
Thiem Van Chu, Ryuichi Kitajima, Kazushi Kawamura, Jaehoon Yu and Masato Motomura

2019, Tianjin, China

Partitioning FPGA-Optimized Systolic Arrays for Fun and Profit
Long Chung Chan, Gurshaant Malik and Nachiket Kapre

2018, Naha, Japan

Dither NN: An Accurate Neural Network with Dithering for Low Bit-Precision Hardware

Kota Ando, Kodai Ueyoshi, Yuka Oba, Kazutoshi Hirose, Ryota Uematsu, Takumi Kudo, Masayuki Ikebe, Tetsuya Asai, Shinya Takamaeda-Yamazaki and Masato Motomura

2017, Melbourne, Australia

Synthesis of Program Binaries into FPGA Accelerators with Runtime Dependence Validation

Shaoyi Cheng, Qijing Huang and John Wawrzynek

2016, Xian, China

High Density, Low Energy, Magnetic Tunnel Junction Based Block RAMs for Memory-rich FPGAs

Kosuke Tatsumura, Sadegh Yazdanshenas and Vaughn Betz

2015, Queenstown, New Zealand

Energy Minimization in the Time-Space Continuum

Hyunseok Park, Shreel Vijayvargiya and André DeHon

2014, Shanghai, China

Design Re-Use for Compile Time Reduction in FPGA High-Level Synthesis Flows

Marcel Gort and Jason Anderson

2013, Kyoto, Japan

Maximum Flow Algorithms for Maximum Observability During FPGA Debug

Eddie Hung, Al-Shahna Jamal and Steven J. E. Wilton

2012, Seoul, South Korea

iDEA: A DSP Block Based FPGA Soft Processor

Hui Yan Cheah, Suhaib A. Fahmy and Douglas L. Maskell

Graph Minor Approach for Application Mapping on CGRAs

Liang Chen; Tulika Mitra

2011, New Delhi, India

[**VLIW-SCORE: Beyond C for Sequential Control of SPICE FPGA Acceleration**](#)
Nachiket Kapre and André DeHon

2010, Beijing, China

[**Parallelizing FPGA placement using transactional memory**](#)
Steven Birk. J. Gregory Steffan and Jason H. Anderson

2009, Sydney, Australia

[**American Option Pricing on Reconfigurable Hardware Using Least-Squares Monte Carlo Method**](#)
Xiang Tian and Khaled Benkrid

2008, Taipei, Taiwan

[**Optimizing Residue Arithmetic on FPGAs**](#)
Haohuan Fu, Oskar Mencer and Wayne Luk

2007, Kitakyushu, Japan

[**Memory Footprint Reduction For FPGA Routing Algorithms**](#)
Scott Y.L. Chin and Steven J.E. Wilton

2006, Bangkok, Thailand

[**FPGA core watermarking based on power signature analysis**](#)
Daniel Ziener and Jurgen Teich

2005, Singapore

[**Dynamic voltage scaling for commercial FPGAs**](#)
C.T. Chow, L.S.M. Tsui, Philip H.W. Leong, Wayne Luk; Steven J.E. Wilton

2004, Brisbane, Australia

[**Directional and Single-Driver Wires in FPGA Interconnect**](#)
Guy Lemieux; Edmund Lee; Marvin Tom; Anthony Yu

2003, Tokyo, Japan

[Product Term Embedded Synthesizable Logic Cores](#)

Andy Yan and S.J.E. Wilton

[Source](#)

ACM TRETS Best Paper Awards

The ACM Transactions on Reconfigurable Technology and Systems (TRETS) has awarded Best Paper Awards to the following papers:

2020

VTR 8: High-performance CAD and Customizable FPGA Architecture Modelling
Kevin E. Murray, Oleg Petelin, Sheng Zhong, Jia Min Wang, Mohamed Eldafrawy, Jean-Philippe Legault, Eugene Sha, Aaron G. Graham, Jean Wu, Matthew J. P. Walker, Hanqing Zeng, Panagiotis Patros, Jason Luu, Kenneth B. Kent and Vaughn Betz

2019

FINN-R: An End-to-End Deep-Learning Framework for Fast Exploration of Quantized Neural Networks
Michaela Blott, Thomas B. Preußer, Nicholas J. Fraser, Giulio Gambardella, Kenneth O'brien, Yaman Umuroglu, Miriam Leeser, Kees Vissers

2018

General-Purpose Computing with Soft GPUs on FPGAs
Muhammed Al Kadi, Benedikt Janssen, Jones Yudi and Michael Huebner

2017

Hoplite: A Deflection-Routed Directional Torus NoC for FPGAs
Nachiket Kapre and Jan Gray

2016

Fine Grained Interconnect Synthesis
Alex Rodionov, David Biancolin and Jonathn Rose.

2015

The Cibola Flight Experiment

Heather Quinn, Diane Roussel-Dupre, Mike Caffrey, Paul Graham, Michael Wirthlin, Keith Morgan, Anthony Salazar, Tony Nelson, Will Howes, Eric Johnson, Jon Johnson, Brian Pratt, Nathan Rollins and Jim Krone

Source