Artifact Evaluation in the FPGA Community

Artifact Evaluation is being adopted in the Computer Science community to further the goals of reproducible research and to improve reliability and confidence of readers in published results. The FPGA community faces specific challenges for producing reproducible results compared to other computing fields due to the use of non-standard hardware platforms.

Miriam Leeser and Suhaib Fahmy led the first Artifact Evaluation effort at FPGA 2020, and have continued to do so every year since then. FPT started evaluating artifacts in 2021 and has continued since then. FCCM introduced artifact evaluation in 2023. ACM TRETS has also introduced artifact evaulation, including for Journal Track papers for FPL and FPT.

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