Artifacts and Open Source

Documenting our artifact evaluation efforts and collecting examples of good open source tools, frameworks, and designs.

- Artifact Evaluation in the FPGA Community
- Evaluated Artifacts

Artifact Evaluation in the FPGA Community

Artifact Evaluation is being adopted in the Computer Science community to further the goals of reproducible research and to improve reliability and confidence of readers in published results. The FPGA community faces specific challenges for producing reproducible results compared to other computing fields due to the use of non-standard hardware platforms.

Miriam Leeser and Suhaib Fahmy led the first Artifact Evaluation effort at FPGA 2020, and have continued to do so every year since then. FPT started evaluating artifacts in 2021 and has continued since then. FCCM introduced artifact evaluation in 2023. ACM TRETS has also introduced artifact evaulation, including for Journal Track papers for FPL and FPT.

Evaluated Artifacts

Here we collect papers with artifacts that have been evaluated and awarded badges at our community conferences and journal. We link the papers, the artifacts, and related repository links for your convenience.

2024

FCCM

LightningSimV2: Faster and Scalable Simulation for High-Level Synthesis via Graph Compilation and Optimization
Rishov Sarkar, Rachel Paul and Cong Callie Hao
[[Artifact]] [Repository]

A Data-Driven, Congestion-Aware and Open-Source Timing-Driven FPGA Placer Accelerated by GPUs
Zhili Xiong, Rachel Selina Rajarathnam and David Z. Pan
[[Artifact]] [Repository]

A Routability-Driven Ultrascale FPGA Macro Placer with Complex Design Constraints
Qin Luo, Xinshi Zang, Qijing Wang, Fangzhou Wang, Evangeline F.Y. Young and Martin D.F. Wong
[[Artifact]] [Repository]

HardCilk: Cilk-like Task Parallelism for FPGAs
Mohamed Shahawy, Canberk Sönmez, Cemalettin Belentepe and Paolo Ienne
[[Artifact]] [Repository]

FPGA

CompressedLUT: An Open Source Tool for Lossless Compression of Lookup Tables for Function Evaluation and Beyond
Alireza Khataei and Kia Bazargan
[Repository]

Hardcaml MSM: A High-Performance Split CPU-FPGA Multi-Scalar Multiplication Engine
Andy Ray, Benjamin Devlin, Fu Yong Quah and Rahul Yesantharao
[

Repository]

Survival of the Fastest: Enabling More Out-of-Order Execution in Dataflow Circuits

Ayatallah Elakhras, Andrea Guerrieri, Lana Josipovic and Paolo Ienne

[Repository]

LevelST: Stream-based Accelerator for Sparse Triangular Solver

Zifan He, Linghao Song, Robert F. Lucas and Jason Cong

[Repository]

Formal Verification of Source-to-Source Transformations for HLS

Louis-Noël Pouchet, Emily Tucker, Niansong Zhang, Hongzheng Chen, Debjit Pal, Gabriel Rodríguez and Zhiru Zhang

[Repository]