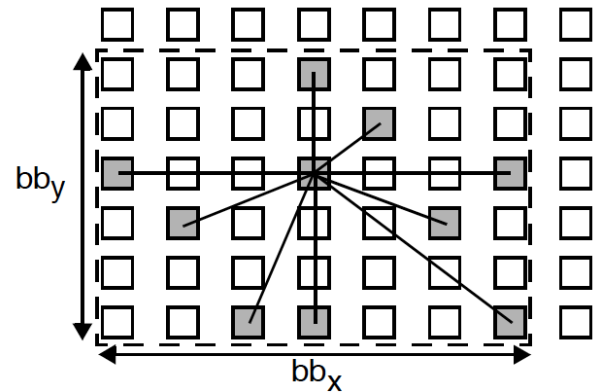# Timing-driven placement for FPGAs

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Year of publication: *2000*
Area: *CAD*

This paper presents the timing-driven placement algorithm used in the most popular open-source FPGA placement and routing system from academia, VPR. Almost every project for new FPGA architecture evaluation has used VPR since its introduction. In addition to its popularity and widespread usage, the T-VPlace algorithm introduced here has three important algorithmic contributions to FPGA timing-driven placement.

- Timing optimization in T-VPlace is carried out by minimizing the weighted sum of the wirelength cost and timing cost in a simulated annealing based optimization engine. The timing cost is measured by the sum of the weighted wirelengths of all nets, where the weight of each net is a polynomial function of the net timing criticality. It was later shown that the criticality-based weighting function used in T-VPlace satisfies the property of asymptotic slack control, which leads to good timing convergence. Moreover, both the wirelength cost and the timing cost in T-VPlace are self-normalized based on the results from the previous iteration, providing great stability to the algorithm.

- This paper shows that the timing slack of each net need not be updated after each cell movement during the iterative placement framework. Accurate path-based timing analysis is applied only periodically, at the end of each temperature iteration in the simulated annealing framework. Using the "stale" slack information did not hurt the timing optimization result but greatly improves the efficiency of the T-VPlace algorithm, although later work shows that this stale slack information does hurt the performance of highly pipelined designs.

- Given the segmented programmable interconnect architecture, the delay between a source-sink pair cannot be estimated simply using its Manhattan distance. However, invoking a detailed router to compute the delay between every source-sink pair during placement is way too costly. Exploiting the symmetry in FPGA architectures, T-VPlace uses a pre-computed delay lookup table, indexed by the distances in the horizontal and vertical directions, to allow fast delay lookup.

These three techniques combined enable T-VPlace to produce high-quality timing optimization results with efficiency. In fact, the first two techniques can also be applied to timing-driven placement for standard cell designs. T-VPlace was a cornerstone in the FPGA place and route system produced by Right Track CAD Corporation, which was acquired by Altera in 2000. The optimization techniques used in T-VPlace have been incorporated into the Altera's FPGA design system Quartus and used by tens of thousands of FPGA designers worldwide.

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