OneChip: An FPGA Processor With Reconfigurable Logic

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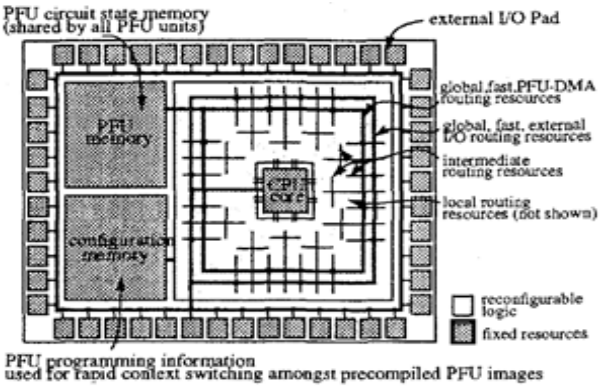

As FPGAs rapidly scaled beyond their initial role of replacing digital glue logic, the idea of using a single chip in a system for everything was very compelling. However, researchers in the reconfigurable computing community continued to find that for some applications a processor was hard to beat. So why not join them?

Ralph Wittig and Paul Chow proposed exactly that in their 1996 OneChip paper. Some prior work in the field (e.g. PAM) had loosely coupled FPGAs and host processors, often limiting performance to achievable communication speed. Alternatively, it had been shown that a small amount of reconfigurable logic could be integrated into a CPU (e.g. PRISC), although the benefits of this customization were small and constrained to mostly simple combinational functions. In contrast, OneChip proposed a tight coupling of a large amount of reconfigurable logic with a microprocessor fabric. In fact, their design showed so much reconfigurable logic in comparison to the CPU core (see figure above) it more accurately could be described as a processor embedded within reconfigurable logic, rather than the inverse.

OneChip not only contained a CPU core within reconfigurable logic, but the reconfigurable logic also appears as a function unit, called a PFU, directly in line with the CPU execute pipeline. Programmable logic placed between the CPU and the chip I/Os enabled a broad range of embedded applications, while tight coupling enabled an order of magnitude speedup or more to be maintained with even a small computation grain size.

This paper not only describes an innovative architecture, but also an innovative prototyping environment that consisted of a multi-FPGA system that leverages both a programmable interconnect chip and pin multiplexing. The architecture also contains an optimized memory interface and register file size to reduce the cost of spilling, showing a speedup of nearly 50 for some cases versus an optimized design. From their architectural design insights, the authors correctly predicted that run-time operating systems that handle context switching would become a major research challenge for the field of reconfigurable computing.

Today, integrated processor cores come standard in available FPGAs and have been one of the major contributing factors in expanding the application space of reconfigurable devices to a large and diverse market space.

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