Configurable Computing Solutions for Automatic Target Recognition

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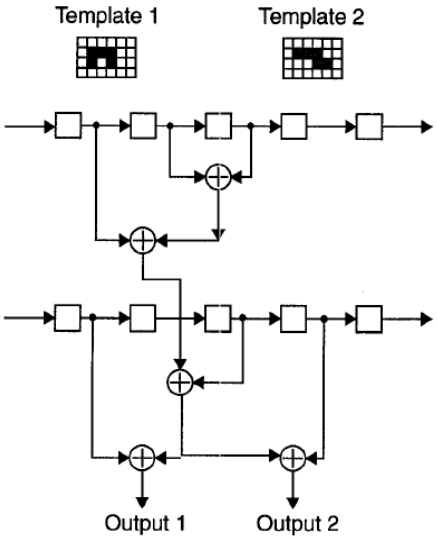

Year of publication: *1996*
Area: *Applications*

In the context of an Automatic Target Recognition application this paper explores computing structures that uniquely exploit FPGA characteristics under the assumption that the FPGA can be rapidly reconfigured. In doing so, this paper was highly influential in raising awareness to the potential of runtime reconfiguration, as evidenced by the citations it has received in the ensuing years.

To address the application, the work described in the paper develops an application-specific CAD system to generate a sequence of optimized circuits that can be sequentially overlaid on the available FPGA resource via rapid reconfiguration. By swapping configuration overlays, the authors overcome the classic performance cliff often encountered in application mapping to FPGA where, beyond a certain size, a circuit no longer fits in the available device and a larger device must be used or the circuit must be radically rearchitected. They also introduced an application-specific common subexpression mapping optimization (see figure) that increased the number of patterns they could pack into one configuration by an order of magnitude.

FPGAs in 1996 were much smaller than they are today and some of the detailed mapping issues discussed in the paper may seem quaint from a modern perspective, but in truth, the fact that implementation details like automatically mapping shift registers to on device memory resources are now handled automatically by FPGA vendor synthesis systems is in part due to pioneering work such as is described in this paper. Today the scale has changed, for instance multipliers are now primitive elements, but at a system level the issues of application mapping and scalability, particularly in real-time image and video processing, are not so different and the contributions of the paper remain relevant.

This paper showed the potential of rapid reconfiguration, but, in the scope of the work it describes, it anticipated the difficulty of bringing such solutions to market. FPGA vendors have been slow to react, but increasingly we are seeing them offering devices and the necessary CAD support that allow applications such as this paper envisioned to enter the mainstream.

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