A Structural Object Programming Model, Architecture, Chip and Tools for Reconfigurable Computing

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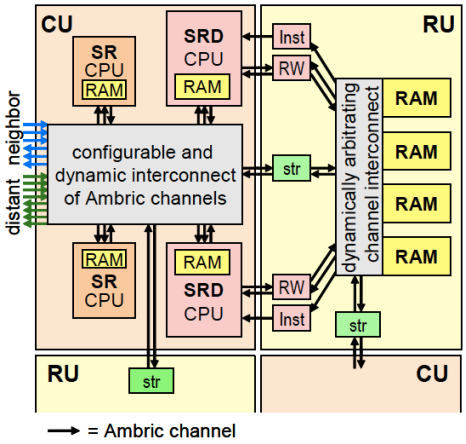

Year of publication: *2007*
Area: *Languages and Compute Models*

This paper is notable for the design, implementation, fabrication and fielding of a production-level, single-chip, coarse-grained reconfigurable computer "Ambric" and associated programming environment (language, compiler, simulator, debugger) based on a formal parallel computation model. The Kahn Process Network model describes a collection of communicating sequential processes in which messages are transmitted over unbounded buffered channels.

Like other coarse-grained architectures, this design foregoes the bit-level flexibility of traditional FPGAs for the energy efficiency of 32-bit word-level operations. However, unlike some coarse-grained designs, the compute module is a full CPU running a clock-cycle-oblivious software program. This design choice solves the application development hurdle of FPGAs and some other ALU-based coarse-grained processor arrays: the applications are written as communicating sequential programs in a Java derivative, and compilation is truly a software compile process − i.e. fast. The architecture supports a reconfigurable, asynchronous communication network. All communication, CPU-to-CPU as well as CPU-to-memory-block, occurs via messages. Communication is expressed graphically in the Eclipse programming environment or in an equivalent textual language, solving the schematic vs. text controversy with the answer "yes." The communication is routed using FPGA-like place and route tools, but since there are a couple of orders of magnitude fewer structured objects than primitive FPGA resources, P&R time is on the order of minutes. The architecture also supports run time reconfiguration.

The ease-of-use dimension is pushed even further with a seamless simulator/debugger and real time visualization of the application running in the simulator or in hardware. In our experience, the visualization environment was invaluable in debugging performance as well as correctness: mismatches in rates between producer and consumer causing performance loss due to stall propagation were clearly visible waves in the data flow displayed in the visualization.

The Ambric chip fabricated in the 2007 timeframe at 130nm was capable of 1 tera-ops/sec of 8-bit operations at 333MHz, consuming less than 15W, an attractive power/performance combination for embedded DSP applications. Unluckily, the economic downturn caught the company, and they did not survive the rough economic roller coaster of the next few years. Yet their design and implementation remain one of the best examples of reconfigurable compute arrays solving the programmability weakness of FPGAs while maintaining high performance.

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DOI: http://dx.doi.org/10.1109/FCCM.2007.7