Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators

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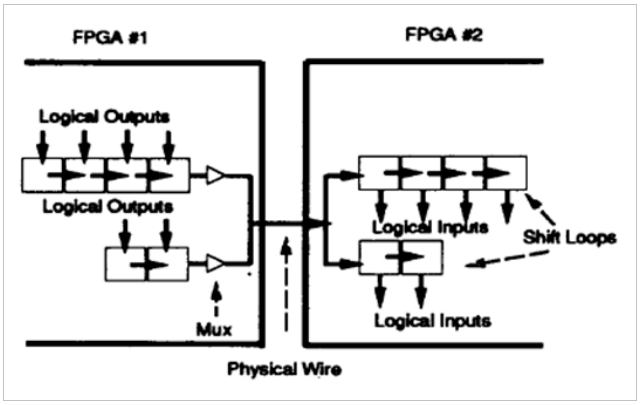

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In the early 1990s, one of the major uses of FPGAs was ASIC emulation. The emulator system could include dozens or hundreds of FPGAs, but each FPGA might be only 10% occupied with logic. The low utilization was a result of the limited pins available for inter-FPGA communication and by the impracticality of re-partitioning and re-routing all those FPGAs for each modification of the ASIC design as it was debugged.

The Virtual Wires work was directed at addressing the FPGA pin limitation with a simple, powerful idea: time-multiplexing the pins, serializing data onto an output pin and de-serializing it at the input. This innovation employed unused logic in the FPGA fabric to implement the serializing and de-serializing. Since logic emulation ran with clock speeds well below the FPGA's capability and since the pin limitation left the FPGAs with excess unused logic, no delay or capacity penalty resulted from Virtual Wires. In fact, emulator systems employing Virtual Wires achieved improved speed and capacity because of their more efficient use of the FPGA logic and pins. To commercialize the idea, the authors founded Virtual Machine Works which was later acquired by IKOS. Understandably, the Virtual Wires concept was quickly adopted by major logic emulator companies.

The paper presents the Virtual Wires concept, describing not only chip-to-chip communication, but the full application in emulators in different topologies. The paper includes the circuit diagram, timing diagram and software flowchart for transforming a large netlist into a virtual wires netlist. The authors further support the idea with a formal analysis of the tradeoffs of deeper multiplexing and a derivation of an optimal partition size.

This paper demonstrated large-scale insertion of custom logic into an FPGA netlist to perform computations in soft logic that the FPGA hardware did not support. It was an "Aha!" moment for many.

The Virtual Wires concept quickly made its way into FPGA hardware. Xilinx implemented hardware assistance for serializing data onto output pins in 1995. Serializers and deserializers have since become standard components of FPGA I/O blocks, and high-speed SERDES blocks of today can trace a lineage back to Virtual Wires and this paper in 1993.

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