Garp: A MIPS Processor with a Reconfigurable Coprocessor

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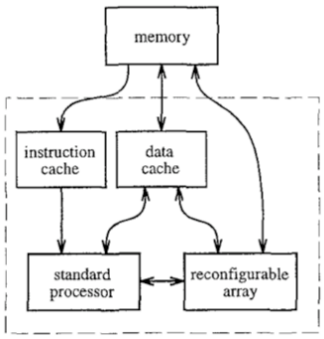

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This paper introduced a novel hybrid architecture that tightly coupled a MIPS processor with a customized reconfigurable array. A programming environment was described that allows a programmer to jointly develop the reconfigurable and sequential portions of an application.

Although there were several good architectural examples of coupled processor/reconfigurable arrays developed prior to this work, Garp provided convincing, quantitative evidence that such an architecture is both technically feasible and offers performance advantages. This paper provides one of the best examples of an FCCM paper that introduces a novel architecture, provides a programming environment, estimates area and delay, and demonstrates the benefits of the architecture and programming environment with speed-up on application examples. Few FCCM papers provide such a convincing demonstration on such a broad set of work.

For good reason, this paper is among the most widely cited papers from FCCM. The concepts introduced in this paper in 1997 address the many of the same challenges facing reconfigurable computing systems today. Some of these concepts are still of interest to modern research in reconfigurable systems. Custom processor instructions were introduced to manage the configuration of the reconfigurable array and data transfer between the processor and the array. A shared memory architecture allowed for high-bandwidth, coherent communication between memory and the processor/array pair. Caching of configuration data allowed for high-speed configuration context switching. A customized reconfigurable fabric facilitated efficient processing of 32-bit data.

This paper inspired many follow-on efforts in both reconfigurable architecture and compilation tools. A fascinating effort was pursued to automatically generate reconfigurable hardware accelerators from traditional software. The tight integration of processor and reconfigurable array within the Garp architecture motivated the need for a unified development environment where all functionality is defined in traditional sequential code. This paper will continue to impact the field of reconfigurable computing for the coming decade.

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